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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,368	02/13/2002	James Harold Lauffenburger	Q-68549	5512

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EXAMINER	
MONBLEAU, DAVIENNE N	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,368	LAUFFENBURGER ET AL.	
	Examiner	Art Unit	
	Davienne Monbleau	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/13/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claims 1 and 16, the phrase "means for balancing" is not clear. Although the specification states that the switching circuitry is the means, there is not adequate explanation to the term "balancing". Since Examiner does not believe this to be a term of art, clarification is required.

Further regarding Claims 1 and 16, it is not clear how the integrating voltage storage device develops a voltage during the reset phase that is equal to said bias voltage, but is then being pulled to a reference potential during the same reset phase.

Regarding Claim 13, the phrase "within the array with the least, respectively the greatest, intensity" is confusing and should be corrected for clarity.

Claims 2-12, 14, 15 and 17-20 are rejected as being dependent on an indefinite base claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, to the extent taught and understood, is rejected under 35 U.S.C. 102(b) as being anticipated by Woolaway (US 5,602,511).

Regarding Claim 1, *Woolaway* discloses in Figure 2 an optical sensor comprising a photodetector (PD), an integrating circuit (10) coupled with the output of the photodetector (PD), said integrating circuit comprising an operational amplifier (AMP) having a non-inverting input connected to a non-zero bias voltage, an inverting input coupled to said photodetector (PD), and at least one output, an integrating voltage storage device (C1) having a first terminal coupled to the operational amplifier (AMP) output and a second terminal coupled to the operational amplifier (AMP) inverting input, and switching circuitry (RESET SW) for controlling timing of the integrating circuit (10) and switching the integrating circuit (10) between a reset phase and an integration phase. *Woolaway* further discloses in column 3 lines 44-45 means for balancing said operational amplifier. Applying a voltage across said integrating voltage storage device is inherent when resetting the circuitry before the subsequent integration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the

various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woolaway (US 5,602,511) in view of Marion et al. (US 6,201,248). *Woolaway* teaches in Figure 2 an integrating voltage storage device but does not teach that said device is a MOS transistor. *Marion* teaches in Figure 2A and in column 3 lines 5-8 that an integrating voltage storage device (CPEL) may be a MOS transistor operating in an accumulation mode for integration. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a MOS transistor in *Woolaway*, as taught by *Marion*, to efficiently convert the current into voltage via integration.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woolaway (US 5,602,511). Woolaway teaches in Figure 2 a photodetector (PD) but does not teach that said photodetector is a reverse-biased photodiode. Lacking any criticality, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a reverse-biased photodiode in *Woolaway*, as the detector, to efficiently detect incident radiation and output an electrical signal.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woolaway (US 5,602,511) in view of Pain (US 6,384,413). *Woolaway* teaches in Figure 2 that said operational amplifier is a differential amplifier but does not teach a pair of transistors

having a half-folded cascode stage. Pain teaches in figure 3 and in column 4 lines 53-61 a readout circuit comprising a differential operational amplifier (50) with a pair of cascode transistors (M3 and M4). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the differential amplifier in *Woolaway*, as taught by *Pain*, to achieve high injection efficiency at high speeds. (See *Pain* column 4 lines 53-55).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woolaway (US 5,602,511) in view of Chen et al. (US 6,128,039). *Woolaway* does not teach a source-follower. *Chen* teaches in Figure 2 a amplifier device comprising an array of detectors (301) and an output buffer stage (310), wherein said output buffer stage may be a source-follower (see column 3 lines 65-67). It would have been obvious to one of ordinary skill in the art to use a source-follower in W*oolaway*, as taught by *Chen*, to further amplify the output signal of the detectors within the array.

Allowable Subject Matter

Claim 16 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claims 2, 3, 7-12, 14 and 17-20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claims 2, 3, and 7-12, the cited prior art of record does not teach or fairly suggest an optical sensor comprising, along with the other claimed features, an

output stage comprising a gate terminal connected to the operational amplifier output and an output terminal connected to said first terminal of the integrating voltage storage device.

Regarding Claim 14, the cited prior art of record does not teach or fairly suggest an optical sensor comprising, along with the other claimed features, a first source-follower output stage with a gate terminal connected to said first terminal of the integrating voltage storage device and a drain terminal connected to a first supply potential and a second source-follower output stage with a gate terminal connected to said operational amplifier output and a drain terminal connected to a second supply potential.

Regarding Claims 16-20, the cited prior art of record does not teach or fairly suggest an integrating circuit comprising, along with the other claimed features, an output stage comprising a gate terminal connected to the operational amplifier output and an output terminal connected to said first terminal of the integrating voltage storage device.

The advantages of these features are in the specification on page 3 lines 13 – 33.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. *Aswell et al.* (US 6,031,217) teaches in Figure 6 an active integrator optical sensor (13) comprising an operational amplifier (50), an integration capacitor (51) that is separate from an offset voltage storage capacitor (54), and switching circuitry (117) to reset the circuit. *Hoffman* (US 6,252,462) teaches in Figure 1 a switch placed across the feedback capacitor to reset/discharge the capacitor when it is closed and then begin the integration time when it is open. *Fowler* (US 6,633,028) teaches in Figure

1 an image sensor array comprising a photodetector (21), an operational amplifier (23), an integrating voltage storage device (24), and a reset switch (25). *Jordanov* (US 6,587,003) teaches in Figure 7 a preamplifier for a detector (162) comprising an amplifier (160), an integrating voltage storage device (166), and a reset control circuit (168). *Wake* et al. (US 6,150,649) teaches in Figure 5 a variable gain amplifier comprising an operational amplifier (46), an integrating voltage storage device (52) and a reset switch (50). *Mizuno* et al. (US 6,642,501) teaches in Figure 3 an amplifier circuit comprising CDS circuits (21 and 22), wherein each CDS circuit comprises an amplifier (A), an integrating voltage storage device (C), and a switch (SW).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Davienne Monbleau whose telephone number is 571-272-1945. The examiner can normally be reached on Mon-Fri 9:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on 571-272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dorienne Monbleau

DNM

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